



DM74197 Presettable Binary Counters

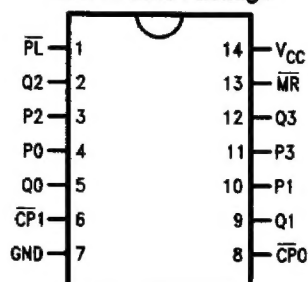
General Description

The '197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The '197 has a Master Reset (\overline{MR}) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (\overline{PL}) overrides

clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when \overline{PL} is LOW and storing the data when \overline{PL} is HIGH.

Connection Diagram

Dual-In-Line Package



TL/F/9784-1

Order Number DM74197N
See NS Package Number N14A

Pin Names	Description
$\overline{CP0}$	$\div 2$ Section Clock Input (Active Falling Edge)
$\overline{CP1}$	$\div 8$ Section Clock Input (Active Falling Edge)
\overline{MR}	Asynchronous Master Reset Input (Active LOW)
P0-P3	Parallel Data Inputs
\overline{PL}	Asynchronous Parallel Load Input (Active LOW)
Q0	$\div 2$ Section Output*
Q1-Q3	$\div 8$ Section Outputs

*Q0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP1}$ input.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM74197			Units
		Min	Nom	Max	
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current			−0.25	mA
I _{OL}	Low Level Output Current			16	mA
T _A	Free Air Operating Temperature	0		70	°C
t _s (H) t _s (L)	Setup Time HIGH or LOW P _n to \overline{PL}	10 15			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW P _n to \overline{PL}	0 0			ns
t _w (H)	$\overline{CP0}$ Pulse Width HIGH	20			ns
t _w (H)	$\overline{CP1}$ Pulse Width HIGH	30			ns
t _w (L)	\overline{PL} Pulse Width LOW	20			ns
t _w (L)	\overline{MR} Pulse Width LOW	15			ns
t _{rec}	Recovery Time \overline{PL} to $\overline{CP_n}$	20			ns
t _{rec}	Recovery Time \overline{MR} to $\overline{CP_n}$	20			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −12 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	2.4	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min		0.2	0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 5.5V, $\overline{CP_1}$			1	mA
		V _{CC} = Max, V _I = 2.4V			40	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			−1.6	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	−18		−57	mA
I _{CC}	Supply Current	V _{CC} = Max, All Inputs = GND			59	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

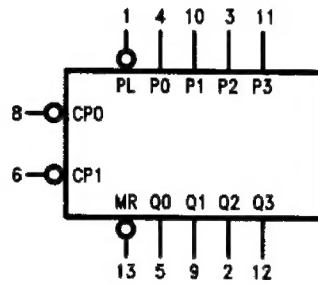
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25^\circ C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C _L = 15 pF		Units
		R _L = 400Ω		
		Min	Max	
f _{max}	Maximum Count Frequency at $\overline{CP0}$	50		MHz
f _{max}	Maximum Count Frequency at CP1	25		MHz
t _{PLH} t _{PHL}	Propagation Delay $\overline{CP0}$ to Q0		12 15	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{CP1}$ to Q1		18 21	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{CP1}$ to Q2		36 42	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{CP1}$ to Q3		54 63	ns
t _{PLH} t _{PHL}	Propagation Delay P _n to Q _n		24 38	ns
t _{PLH} t _{PHL}	Propagation Delay \overline{PL} to Q _n		33 36	ns
t _{PHL}	Propagation Delay MR to Q _n		37	ns


Logic Symbol



$V_{CC} = \text{Pin } 14$
 $GND = \text{Pin } 7$

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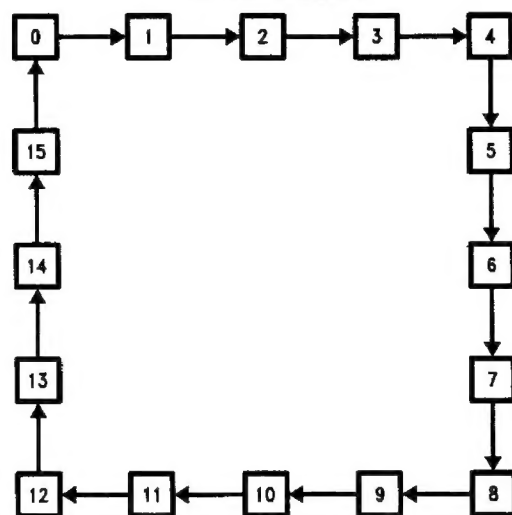
Mode Selection Table

Inputs			Response
\overline{MR}	\overline{PL}	\overline{CP}	
L	X	X	Q_n Forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H		Count Up

H = HIGH Voltage Level

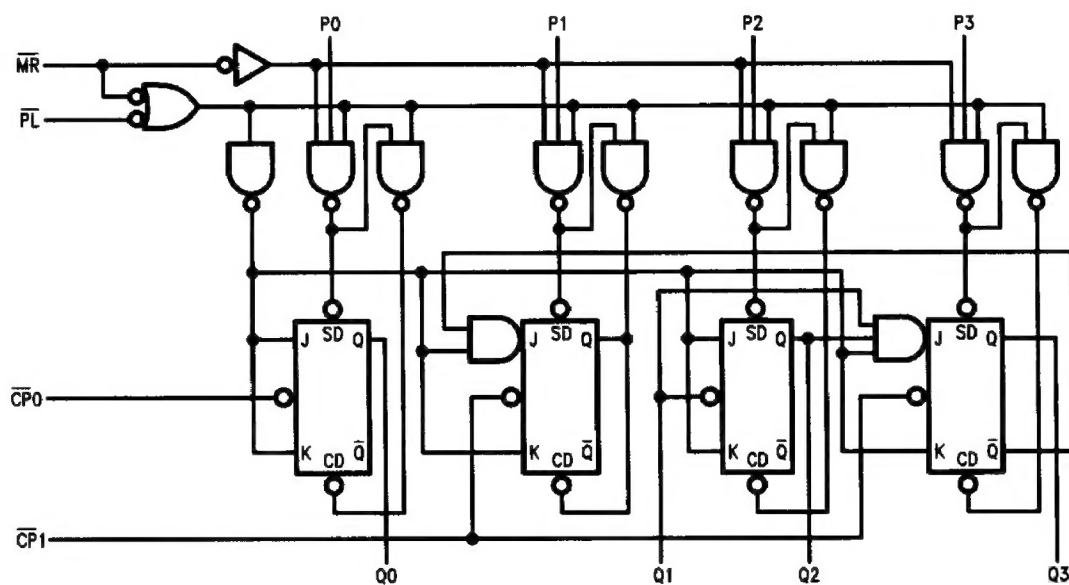
L = LOW Voltage Level

X = Immaterial

 $\div 16$ State Diagram

TL/F/9784-3

Logic Diagram



TL/F/9784-4